Mixed-Criticality-Cluster at DIF2017

Modern embedded applications already integrate a multitude of functionalities with potentially different criticality levels into a single system and this trend is expected to grow in the near future. Further, Europe is facing a challenge with the advent of multicore and the potential to integrate in a single platform systems with different levels of dependability and security, known as mixed-criticality systems integration. Without appropriate preconditions, the integration of mixed-criticality subsystems based on multi- and many-core processors can lead to a significant and potentially unacceptable increase of engineering and certification costs.

The European projects DREAMS and SAFEPOWER collaborate in an European Mixed-Criticality Cluster (MCC) and closely work together in terms of identification of future challenges in the design and development of mixed-criticality multicore systems, join dissemination activities, and where possible exploring techniques to attach those challenges.

These two European projects presented their technologies at the Digital Innovation Forum (DIF) 2017 in Amsterdam. This international event was the industry-driven digital innovation conference in the Europe, showing research and innovation results and emerging challenges towards a vision on the future for the industry. DIF 2017 took place on 10th and 11th of May 2017 in the RAI in Amsterdam, Netherlands.

Figure 1 Mixed-Criticality Cluster at DIF2017

Distributed REal-time Architecture for Mixed-criticality Systems

The FP7-ICT integrated project DREAMS started on October 1st 2013 and aims at developing a cross-domain architecture and design tools for networked multi-core chips, where the execution of the application subsystems of different criticalities is supported.

The ambitious goals of the project are targeted and supported by 16 project partners distributed across six European countries. The project partners include major European companies encompassing large enterprises (Alstom, STMicroelectronics, Thales, TÜV Rheinland) and SMEs (FENTISS, Real-Time-at-Work, TTTech, Virtual Open Systems). Furthermore, leading universities and research institutes (FORTISS, IKERLAN, ONERA, polytechnic university of Valencia, SINTEF, technological educational institute of Crete, technical university of Kaiserslautern and university of Siegen) contribute to this four-year project.

In April 2017, DREAMS partners came together in Munich to have another face-to-face meeting before the end of the project. The aim of this meeting was to discuss the current status of the project and to address the recommendations from the last review meeting in order to improve the project results. Moreover, there was a detailed discussion about the final demonstration which takes place at the final review meeting.

DREAMS partners organize a summer-school on mixed-criticality applications and systems that will take place from 25th to 28th of September 2017 in Valencia, Spain. This summer-school is hosted by polytechnic university of Valencia and focuses on Mixed-criticality architectures and platforms. The aim is to provide the students with background and insight, which is hard to attain from the papers in the domain of mixed-criticality systems by offering a combination of lectures and practical student work.

After an intensive work during the past three years, the DREAMS partners prepare themselves for the next review meeting taking place late 2017. This meeting is going to be the final review meeting and will take place at the end of the project (in October or November 2017). The aim of this meeting will be the reviewing of the project objectives and there will be demonstrations of the DREAMS technologies as well as the avionic, healthcare and windpower use cases.

For more information cf. http://dreams-project.eu/.

SAFEPOWER

Safe and secure mixed-criticality systems with low power requirements

On May 16-18, 2017 the SAFEPOWER mid-project meeting was held at the KTH premises in Stockholm, Sweden. The SAFEPOWER project aims to enable the development of mixed-criticality systems with low power, low energy and low temperature in combination with safety, and real-time through the provision of a reference architecture, platforms and tools to facilitate the development, testing and validation of these kinds of systems. It is expected that the SAFEPOWER reference architecture and platforms will enable the integration and partitioning of mixed-criticality applications on a single device while reducing the total power consumption by 50% compared to the non-integrated multi-chip implementation.

In this meeting the partners were able to consolidate a first set of project tools incorporating SAFEPOWER technology and report on the progress of their integration within the industrial railway and avionics demonstrators leaded by CAF-Signalling and CAF. The project approach has also received a positive assessment by a certification authority with regard to the technical compliance of the technology in the context of safety standards (IEC-61508).

Figure 2 SAFEPOWER Team in the Stockholm meeting

Critical Real-Time Embedded Systems (CRTES) such as railway, aerospace, automotive and energy generation systems face a disruptive challenge caused by the massive irruption of mixed-criticality systems based on multicore processors. At the same time low-power is an intensifying demand in many market segments, a competitive advantage for CRTES that have to operate with limited energy (e.g., battery powered systems), an enabler for higher availability and a desired feature towards near-zero emission in systems with tens/hundreds of

devices. Power is also a key aspect in mixed-criticality systems as another resource (together with time and space) that has to be shared among different applications and has to be strictly controlled not to cause undesired interferences.

SAFEPOWER builds a comprehensive suite of multi-core platform technologies as well as analysis, simulation and verification tools for low-power mixed-criticality systems, including hardware and software reference platforms assisting the implementation, observation and test of such applications. This includes IMPERAS' OVP technology extended to cover the multicore, power estimation and safety analysis requirements of the project in simulation time and FentISS' XtratuM hypervisor as the handler of all safety and power related services on runtime.

SAFEPOWER project is funded by the EU H2020 program under grant agreement No 687902 with 3.62 million Euros. It has a budget of four million euros and an execution period of 36 months. Besides IK4-IKERLAN (ES) as coordinator, the following organizations participate in the project: UNIVERSITAET SIEGEN (DE), OFFIS (DE), CAF SIGNALLING (ES), FentISS (ES), IMPERAS (UK), SAAB (SE), and KUNGLIGA TEKNISKA HOEGSKOLAN (SE). This research work will contribute to strengthen the leadership and excellence of Europe in the development of reference architectures and tools for the CRTES.

For more information cf. http://safepower-project.eu/.