

Distributed REal-time Architecture for Mixed criticality Systems (DREAMS)

A large, stylized red ladder is positioned on the left side of the slide. A red stick figure is climbing the ladder, with its arms raised in a celebratory gesture. The ladder has five visible rungs.

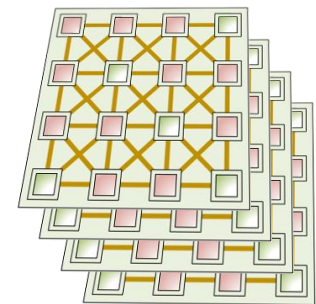
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University of Siegen*

- Pressing requirement to reduce the number of computers and cables
- Mixed-criticality systems integrate functions with different importance and safety levels
- Trend to multi-core platforms due to limited scalability of uniprocessors

Mixed-Criticality in Many Application Domains



Networked Multi-Core Chips



- Modular certification of mixed-criticality systems
- Platforms for mixed-criticality systems and resource guarantees (multi-core processors, I/O, networks, memory)
- Development methodologies with support for design space exploration, scheduling and timing analysis
- Heterogeneous models of computation
- End-to-end systems engineering addressing significant extra functional properties (e.g., time, energy and power budgets, reliability, safety, security)

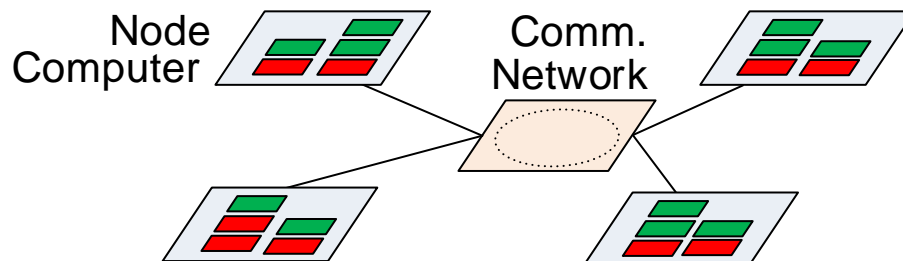
- Project full title: Distributed REal-time Architecture for Mixed criticality Systems
- Project duration: October 1, 2013 – Sept. 30, 2017
- Type of project: Integrated Project (IP)
- Budget Total: 15.5 mill. EUR

Industry	Thales SA	France
	Alstom Wind S.L.	Spain
	STMicroelectronics	France
	TÜV Rheinland	Germany
SME	TTTech	Austria
	RealTime-At-Work	France
	Virtual Open Systems	France
	FENTISS	Spain

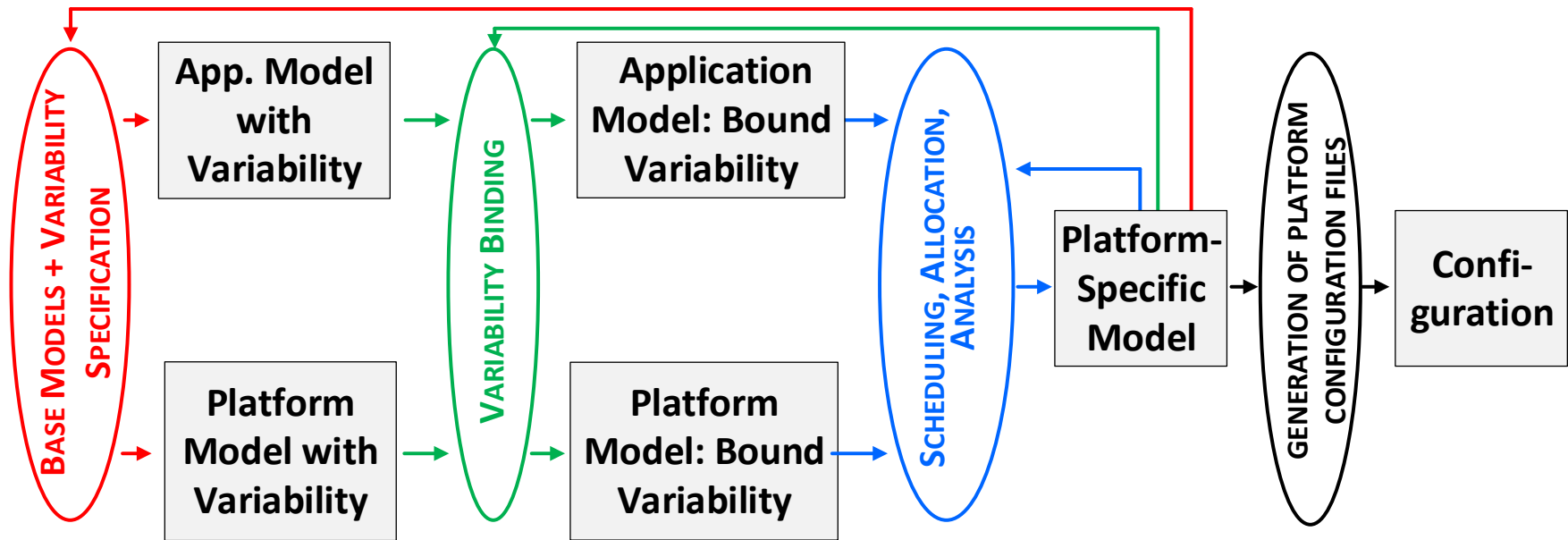
Research Org.	ONERA	France
	Ikerlan	Spain
	SINTEF	Norway
	Fortiss	Germany
Univ.	Universität Siegen	Germany
	TU Kaiserslautern	Germany
	UPV	Spain
	TEI	Greece

Mixed-criticality architecture for networked multi-core chips

1. Architectural style and modelling methods
2. Virtualization technologies for security, safety, real-time
3. Adaptation strategies for mixed-criticality systems
4. Model-driven development methodology and tools
5. Modular certification and mixed-criticality product lines
6. Feasibility of DREAMS architecture in real-world scenarios
7. Promoting widespread adoption and community building

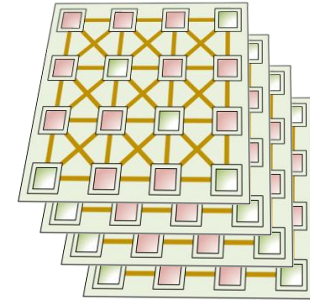


- Architecture style for seamless virtualization of networked embedded platforms with support for security, safety and real-time performance
- *Models of hierarchical platforms* comprised of networked multi-core chips to enable MDE
- *Development process* ranging from modelling and design to validation of mixed-criticality systems

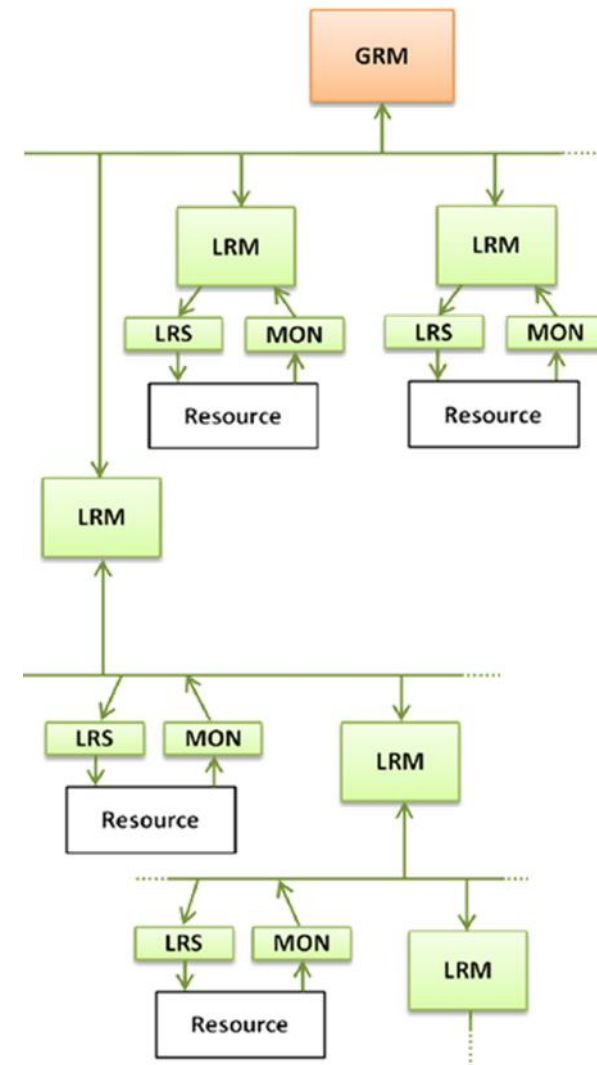


- Certifiable platform services for virtualization and *segregation of resources at cluster and chip-level*
 - ◆ I/O virtualization
 - ◆ Processor virtualization using hypervisors
 - ◆ Message-based networks and memory architectures
 - ◆ Dynamic resource management
- *Gateways* for end-to-end segregation as means for integration of mixed criticalities at chip-, network- and cluster-level
- Support for *monitoring and dynamic configuration*

Networked Multi-Core Chips



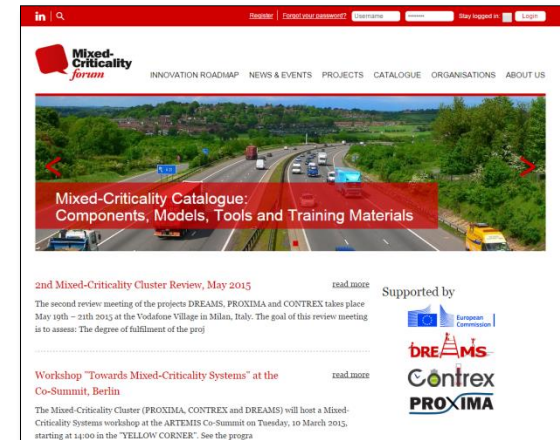
- Support for *system wide, high level constraints*, such as end-to-end deadlines and reliability
- Combination of global strategies with local monitoring and management
 - ◆ *Monitor (MON)* for monitoring different resource types (e.g., availability, timing)
 - ◆ *Global Resource Manager (GRM)* for global decisions with information from monitors
 - ◆ *Local Resource Manager (LRM)* for local decisions and resource abstractions
 - ◆ *Local Resource Schedulers (LRS)* performs runtime scheduling of resource requests (e.g., execution on processor, memory)



- Avionic demonstrator: avionics display with different levels of criticality
- Wind power demonstrator: Wind turbine control system combining safety-critical application for the pitch control with non safety-criticals services
- Healthcare demonstrator: body gateway for a remote patient monitoring application



1. *Website* for mixed-criticality community with results provided by several projects (DREAMS, PROXIMA, CONTREX, CRYSTAL, EMC2, RECOMP)
2. Organization of *community building events* (e.g., community building activity at HIPEAC 2015 attracted more than 50 participants to discuss future directions of MCS)
3. Joint *standardization* activities
4. Facilitate *information flow* and interfaces between projects
5. *Training* of community
6. *Innovation roadmap* for MCS



MixedCriticalityForum.org



HIPEAC Workshop, Jan 2015

- Leverage multi-core platforms for a system perspective of mixed-criticality systems combining the chip-level and cluster-level
- Reduced development cost and time-to-market for MCS
- Exploitation of economies of scale
- Consolidation and integration of virtualization solutions and development methods from previous projects
- Flexibility, adaptability and energy efficiency through integrated resource management
- Higher reliability, security and safety

